CLAIMS

1. (Currently amended) An amplifier comprising:

an input terminal to receive an input signal;

a first gain stage comprising a pair of input transistors;

a second gain stage to drive ~~an~~ a pair of output stages;

a first resistor coupled between emitters of the pair of input transistors;

the pair of output stages to provide inverting and non-inverting differential output signals on inverting and non-inverting output nodes; and

a pair of feedback resistors ~~signal~~ electrically connected between the inverting and non-inverting output nodes ~~to~~ and the emitters of the input transistors ~~through a resistor network.~~, wherein the feedback resistors are sized so that signal current through the first resistor is provided primarily by the output stages.

2. (Withdrawn—currently amended) The amplifier of claim 1, wherein the first resistor ~~network comprising resistor having~~ and the pair of feedback resistors have values chosen to provide equal gain magnitude to the inverting and non-inverting output nodes from a single-ended input.

3. (Currently amended) The amplifier of claim 1, the amplifier further comprising a third feedback resistor electrically connected between the inverting output node and the input terminal to synthesize an input impedance.

4. (Original) The amplifier of claim 1, the input terminal being electrically connected to a ferrite bead.

5. (Canceled)

6. (Withdrawn) The amplifier of claim 1, the second gain stage further comprising a common emitter amplifier.

7. (Withdrawn) The amplifier of claim 6, the amplifier further comprising an emitter follower driving the second gain stage.

8. (Withdrawn—currently amended) The amplifier of claim 1, each of the output stages further comprising a constant product loop.

9. (Withdrawn—currently amended) The amplifier of claim 1, each of the output stages further comprising a rail-to-rail output stage.

10. (Withdrawn) The amplifier of claim 1, the amplifier further comprising a non-linear current source electrically connected to an output transistor on a first side of the amplifier and controlled by the opposite side output signal.

11. (Withdrawn) An amplifier, comprising:

an input terminal to receive a single input signal;

a first opposite side comprising a non-inverting output node to provide a non-inverting output signal;

a second opposite side comprising an inverting output node to provide an inverting output signal; and

a second gain stage current source biased dynamically dependent upon the opposite side output signal.

12. (Withdrawn) The amplifier of claim 11, the first stage further comprising a pair of differential transistors having emitters electrically coupled to the high output node through a feedback resistor network.

13. (Currently amended) An amplifier, comprising:

an input terminal to receive an input signal;

a first gain stage comprising a pair of input transistors;

a first resistor coupled between emitters of the pair of input transistors;

~~an~~ a pair of output stages coupled to the pair of input transistors to provide [[an]] inverting and non-inverting differential output signals on inverting and non-inverting output nodes; and

a pair of feedback resistors ~~signal~~ electrically connected between the inverting and non-inverting output nodes ~~to~~ and the emitters of the input transistors ~~through a resistor network.~~, wherein the feedback resistors are sized so that signal current through the first resistor is provided primarily by the output stages.

14. (Currently amended) The amplifier of claim 13, the amplifier comprising a second gain stage, wherein the second gain stage ~~drives the output~~ comprises two emitter-follower transistors coupled between the input stage and the pair of output stages.

15. (Withdrawn) A selectable-gain amplifier comprising:

an attenuator having an input terminal and a plurality of output terminals, wherein the attenuator is constructed to generate a plurality of output signals at the output terminals responsive to an input signal received an the input terminal; and

a selection stage coupled to the attenuator and arranged to select one of the plurality of output signals responsive to a gain control signal.

16. (Withdrawn) The amplifier of claim 15 wherein the selection stage comprises a plurality of gm cells.

17. (Withdrawn) A variable gain amplifier comprising:

an attenuator having a plurality of pairs of tap points; and

a plurality of pairs of gm cells, wherein each pair of gm cells is coupled to a corresponding pair of the tap points.

18. (Withdrawn) The amplifier of claim 17 wherein each pair of gm cells is constructed and arranged to operate as a multi-tanh cell.

19. (Withdrawn) An integrated circuit comprising:

a bipolar junction transistor arranged to operate as a saturating switch;

wherein the transistor is dielectrically isolated.

20. (New) The amplifier of claim 13, wherein the pair of output stages comprises a pair of simple gain stages.